MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 2, 2022/2023

PDS0101 – INTRODUCTION TO DIGITAL SYSTEMS

(All sections / Groups)

03 JULY 2023
9.00 AM – 11.00 AM
(2 Hours)

INSTRUCTIONS TO STUDENTS

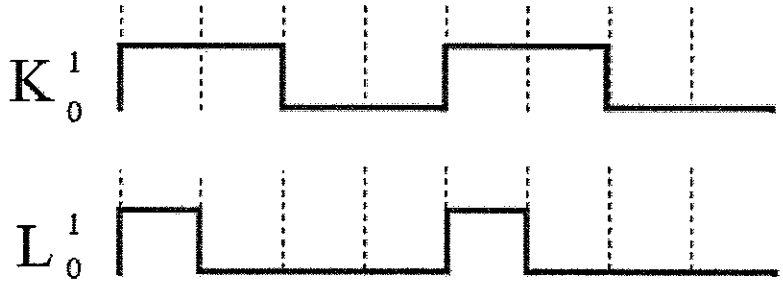
1. This Question paper consists of 7 pages excluding Cover with 5 Questions only.

2. Answer **ALL** Five questions. All questions carry equal marks and the distribution of the marks for each question is given.

3. Please write all your answers in this Question Booklet and submit this Booklet at the end of Examination.

QUESTION 1

a) Referring to the waveforms K and L shown below, identify the value of [3 Marks]

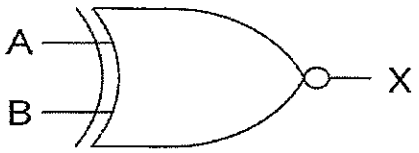


i. pulse width for waveform K and L,
ii. period for waveform K and L,
iii. duty cycle for waveform K and L.

b) Perform the calculation of -83 – 40 using 8-bits signed 2's complement binary numbers and provide your answer in Hexadecimal. [4 Marks]

Continued .....

c) Develop the timing diagram based on the given logic symbol for all the possible input combinations. [3 Marks]



QUESTION 2

a) Simplify the following equation with Boolean algebra. [5 Marks]

$$(A + B)\overline{(BC)} + \overline{(A\bar{B}C)}$$

Continued .....

b) Draw the logic circuit of the answer in (a). [1 Marks]

c) With Boolean Expression, find the standard SOP for the following equation. [4 Marks]

$$(A+B)\overline{(BC)}+\overline{(\bar{B}C)}$$

QUESTION 3

a) With K-Map, find the simplest form of SOP for the following equation. [6 Marks]

$$(A+B)\overline{(AC)}+\overline{(AC)}(B\bar{C})$$

Continued .....

b) Draw a 4-bit parallel adder using one half-adder and three full-adder to perform the addition on 1101 and 1001. [4 Marks]

QUESTION 4

Design a synchronous counter using negative-edge JK flip flop based on the sequence listed below:

100, 010, 001, 111 and repeats.
Those undesired states go to 4 (FOUR) on the next clock pulse.

Your design should include:

a) State Transition Diagram by showing all states. [2 Marks]

Continued .....

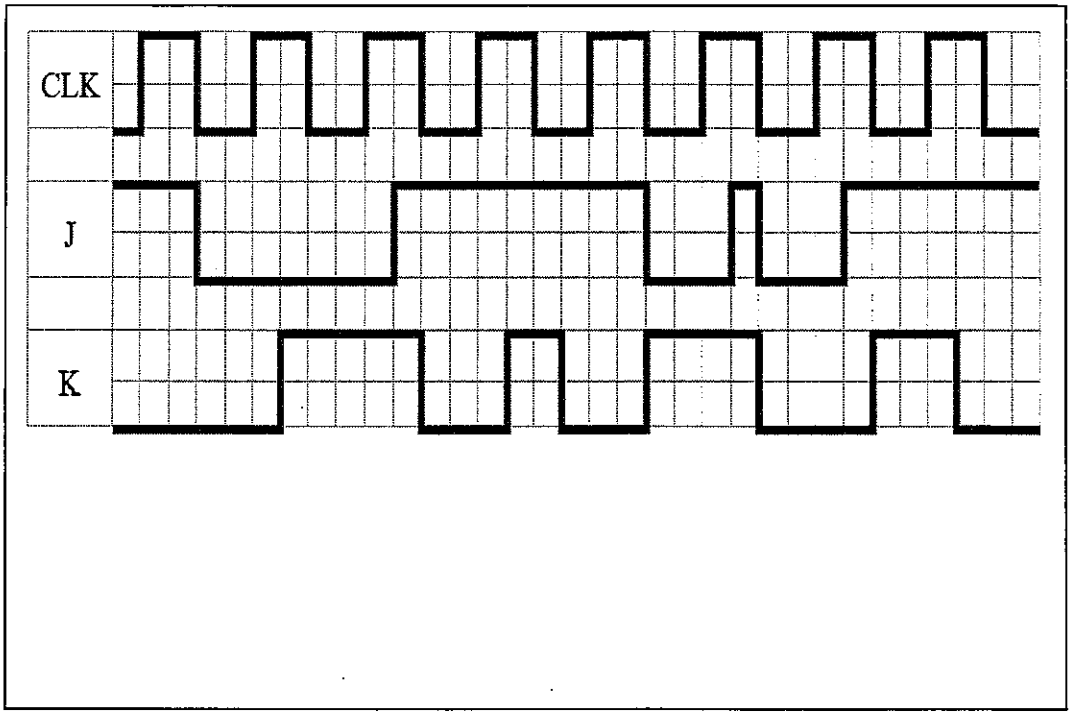
b) By referring to JK flip flop Excitation Table, construct the Next State Table. [4 Marks]

c) Perform Karnaugh Map simplification for each of JK flip-flops inputs. [4 Marks]

Continued .....

QUESTION 5

a) For a negative edge triggered (*NGT*) J-K flip-flop with inputs as shown below, determine the Q output relative to the clock assuming that Q is initially *HIGH. Draw* a timing diagram to represent the output. Make sure you have vertical lines to show the edge triggered. [5 Marks]

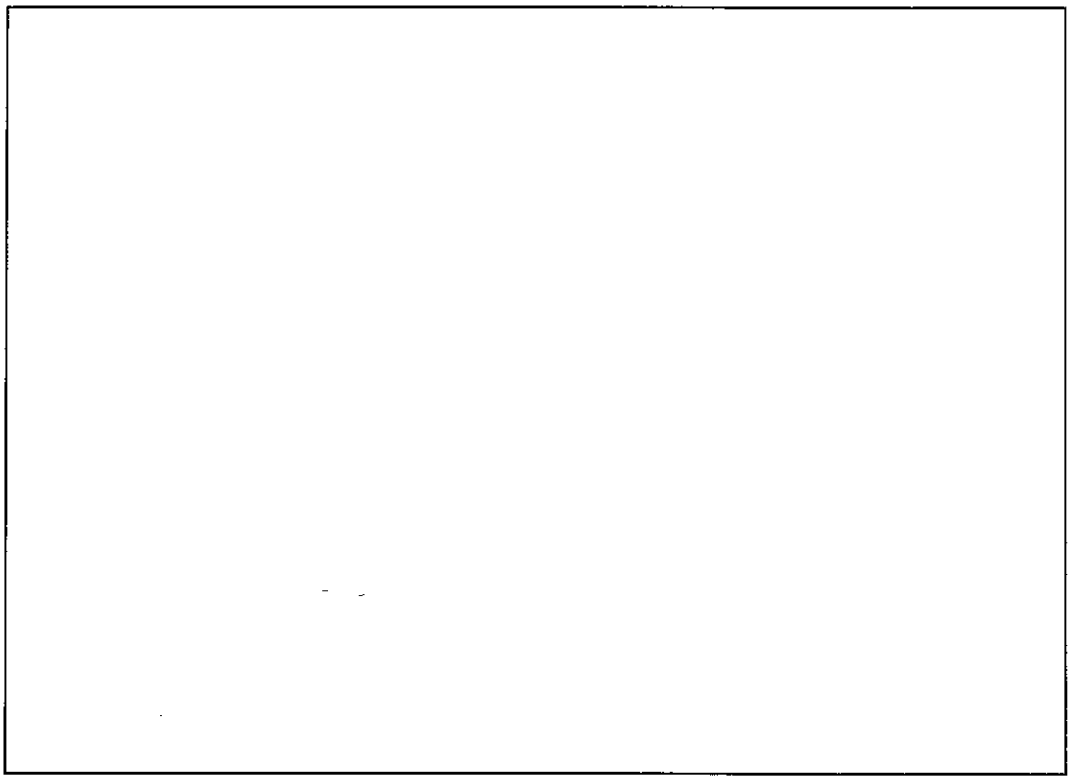


b) Design a 4-bit Johnson counter by performing the following steps.

i. List out the 4-bit Johnson Sequence with the initial sequence of 0101. [2.5 Marks]

Continued .....

ii. Draw a Modulus 8 Johnson counter using D flop-flop. [2.5 Marks]



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